Amendments to the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1-12. (Cancelled)

13. (Currently Amended) A multilayer ceramic substrate comprising:

a ceramic substrate;

a first conductive pattern having a convex via having a step and thereby having only two different widths, and being formed on said ceramic substrate by a transfer printing technology through an intaglio printing using a flexible resin substance;

an insulation layer formed on said first conductive pattern; and

a second conductive pattern electrically connected by way of said via.

14. (Currently Amended) A multilayer ceramic substrate comprising:

a ceramic substrate;

a first conductive pattern and a third conductive pattern each having a convex via having a step and thereby having only two different widths, and being formed on said ceramic substrate by a transfer printing technology through an intaglio printing using a flexible resin substance;

an insulation layer formed respectively o said first and third conductive patterns; and

a second conductive pattern and a fourth conductive pattern each electrically connected with said first conductive pattern and said third conductive pattern, respectively, by way of said via.

15. (Previously Presented) The multilayer ceramic substrate of claim 13, wherein a meshed pattern is provided in a part of said conductive pattern.

16. (Previously Presented) The multilayer ceramic substrate of claim 13, wherein a shield pattern is provided at an outer edge of said conductive pattern.

17. (Previously Presented) The multilayer ceramic substrate of claim 13, wherein said ceramic substrate is provided with a through hole filled with an electroconductive substance and burned, and said via is disposed on the through hole.

18. (Previously Presented) The multilayer ceramic substrate of claim 13, further comprising a dielectric layer formed on a part of said ceramic substrate.

19. (Previously Presented) The multilayer ceramic substrate of claim 13, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected.

20. (Previously Presented) The multilayer ceramic substrate of claim 13, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through an electroconductive paste applied on the top of a fine bump provided on one of said first and second conductive patterns, said fine bump formed by using a second groove which is disposed on said intaglio at a place corresponding to a pad of said LSI chip.

21. (Previously Presented) The multilayer ceramic substrate of claim 13, further comprising an LSI package mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through a lattice of lands with a pitch of not larger than 0.8mm, said lattice provided on one of said first and second conductive patterns.

22. (Previously Presented) The multilayer ceramic substrate of claim 14, wherein a meshed pattern is provided in a part of said conductive pattern.

23. (Previously Presented) The multilayer ceramic substrate of claim 14, wherein a shield pattern is provided at an outer edge of said conductive pattern.

24. (Previously Presented) The multilayer ceramic substrate of claim 14, wherein said ceramic substrate is provided with a through hole filled with an electroconductive substance and burned, and said via is disposed on the through hole.

25. (Previously Presented) The multilayer ceramic substrate of claim 14, further comprising a dielectric layer formed on a part of said ceramic substrate.

26. (Previously Presented) The multilayer ceramic substrate of claim 14, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected.

27. (Previously Presented) The multilayer ceramic substrate of claim 14, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through an electroconductive paste applied on the top of a fine bump provided on one of said first and second conductive patterns, said fine bump formed by using a second groove which is disposed on said intaglio at a place corresponding to a pad of said LSI chip.

28. (Previously Presented) The multilayer ceramic substrate of claim 14, further comprising an LSI package mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through a lattice of lands with a pitch of not larger than 0.8mm, said lattice provided on one of said first and second conductive patterns.